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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,534	11/06/2003	James William Kretchmer	134765	8161

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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,534	KRETCHMER ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-17 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-17 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Applicants' cancellation to claims 2, 3, 18 and 19 is acknowledged. Claims 1, 4-17 and 20-27 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4, 5, 7, 10-13, 15-17 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lucas et al. (US 6,294,820).

In re claims 1, 4, 5 and 10, Lucas et al. teach a method for optical and electrical isolation between adjacent integrated devices (see Fig.1), the method comprising:

- forming at least one trench through an exposed surface of a *SiC* semiconductor wafer 12 (col. 3, lines 29-33) by removing a portion of the semiconductor wafer material 12;
- forming by thermally *growing* an electrically insulating layer 14 (i.e. silicon *oxide,* col. 3, lines 37-39) on the sidewalls and the bottom of the at least one trench;
- filling the at least one trench by conformally depositing an optically isolating material 16, wherein the optically isolating material 16 comprises a *polysilicon*, i.e. a polysilicon layer in polysilicon buffer LOCOS method (col. 3, lines 45-48); and

- planarizing the semiconductor wafer surface by removing the portion of the optically isolating material 16 above the exposed surface of the semiconductor wafer 12 using a CMP technique (col. 3, lines 42-43).

In re claim 7, Lucas et al. teach that the optically isolating material 16 comprises an opaque material since the optically isolating material 16 comprises a polysilicon (col. 3, lines 45-48).

In re claim 11, Lucas et al. teach that the electrically insulating layer 14 comprises silicon oxide and the optically isolating material 16 comprises a polysilicon.

In re claim 12, Lucas et al. teach that the at least trench 14/16 is located between a plurality of adjacent device sites 18/20/22 (Fig.6).

In re claim 13, Lucas et al. teach that the step of forming the at least trench comprises selectively etching the semiconductor wafer 12 with reactive ion etching (RIE) process (col. 3, lines 34-35).

In re claims 15-16, Lucas et al. teach planarizing the semiconductor wafer by subjecting the portion of the optically isolating material 16 above the exposed surface of the semiconductor wafer 12 to an etching process, wherein the planarization can be performed by CMP process (col. 3, lines 42-43).

In re claim 17, Lucas et al. teach a microelectronic device comprising:

- at least two integrated devices 18/20/22, wherein the at least two integrated devices are located in a substrate 12; and
- at least one trench the substrate, wherein the at least one trench physically separates the at least two integrated devices 18/20/22, and the inside of the at least one trench is

coated with an electrically insulating material 14 and filled with an optically isolating material 16 that is conformally deposited (Fig.6).

In re claim 20, Lucas et al. teach that the electrically insulating layer 14 is a thermally grown silicon oxide.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lucas et al. (US '820) in view of Seitz (US 2003/0013270).

Lucas et al disclose growing an oxide as the electrically insulating layer 14 but do not teach depositing a silicon nitride as the electrically insulating layer.

Seitz, however, discloses forming at least a trench 215 in a SiC substrate 212; depositing a silicon nitride liner 228 in the trench 215, wherein the nitride 228 acts as the electrically insulating layer and filling the trench with an oxide layer 216, which acts as the optically isolating material.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to substitute the grown oxide of Lucas with silicon nitride, as taught by Seitz, as the electrically insulating layer, since silicon nitride is an art-recognized equivalent electrically insulating material as opposed to silicon oxide.

6. Claims 8, 9 , 21, 23 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lucas et al. (US '820) in view of Wensley et al. (US 2004/0175897).

In re claims 9, 21 and 23, Lucas et al. do not expressly teach that polysilicon is formed by LPCVD technique.

However, using LPCVD for depositing polysilicon in the trench has been widely used in the art, as evidenced by Wensley et al. (paragraph [0031]), wherein Wensley et al. teach forming a trench 108 in a SiC substrate 106; forming an electrically insulating layer 110 in the trench 108 and filling the trench 108 with polysilicon 112.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use LPCVD technique for depositing polysilicon in the trench, as taught by Wensley et al., in the method of Lucas, since LPCVD is a good candidate for filling polysilicon in the trench.

In re claims 8 and 24, these claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

In re claims 25-27, the teachings of Lucas et al. is illustrative rather than restrictive (col. 6, line 66 through col. 7, line 7). One of the ordinary skill in the art would have been motivated to apply the teachings of Lucas et al. to form the trench isolation in the applications of photodiodes, photoemitters and an array of serially connected diodes.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lucas et al. (US '820) in view of Takaishi (US 6,239,001).

Lucas et al. teach using a polysilicon buffer LOCOS method for forming the optically isolating material (col. 3, line 48) but is silent as to oxidizing the portion of the optically isolating material above the exposed surface of the semiconductor wafer and removing the oxidized portion of the optically isolating material.

However, polysilicon buffer LOCOS method comprises forming a polysilicon layer in the trench followed by a thermal oxidation process (i.e. local oxidation) to convert the polysilicon layer into an oxide. In particular, Takaishi teaches using the polysilicon buffer LOCOS method comprising forming a polysilicon in the trench; oxidizing the portion of the polysilicon, which is equivalent to the claimed optically isolating material, and removing the oxidized portion of the optically isolating material to form a semiconductor device, such as a transistor (col. 1, lines 30-44).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to comprehend that using the polysilicon buffer LOCOS method of Lucas et al. would involve oxidizing the portion of the polysilicon, as taught by Takaishi. In addition, one of the ordinary skill in the art would have been motivated to further removing the

oxidized portion of the polysilicon to provide a ground for forming a semiconductor device, as suggested by Takaishi, since by doing so it would benefit the subsequent processing step,

Response to Arguments

8. Applicant's arguments filed 6/20/2005 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made, as stated previously.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (7:30 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

August 31, 2005

HSIEN-MING LEE
PRIMARY EXAMINER